AMENDMENTS TO THE DRAWINGS

Replacement Drawing Fig. 1A and New Sheet Fig. 1B

Attachment: 2 Sheets of Drawings

REMARKS

Claims 1-33 are all the claims pending in the application. Claims 1-25 are rejected. Claims 26-33 are withdrawn from consideration and have been cancelled. No claims are amended, as the currently claimed invention clearly distinguishes over the prior art.

Drawings

The drawings are objected to under 37 CFR 1.83(a) because the drawings fail to show every feature of the invention specified in the claims. The Examiner states that "the making a transistor having first and second electrodes, a semiconductive layer, and a dielectric layer; said semiconductive layer comprising a semiconductive polymer and said dielectric layer comprising an insulating polymer must be shown or the feature(s) canceled from the claim(s)."

Applicants are submitting a new figure showing an example of the combination of claim features, as identified by the Examiner.

Applicants also are amending the specification at pages 41-43 to add the reference characters shown in the new Figure. The text of the original PCT specification that is the international priority filing for the above referenced US application clearly demonstrates that the proposed new figure is based on the original specification.

Claim Rejections - 35 USC § 102

Claims 1, 2, 4-12, 15-17, 20, 21 and 23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirai (US 7037767 B2). This rejection is traversed for at least the following reasons.

Claim 1

The Examiner asserts that Hirai teaches a method of making a transistor, as claimed, where the step of "depositing on the first electrode a layer of a solution containing material for forming the semiconductive layer and material for forming the dielectric layer" is taught at column 15, lines 17-23. The Examiner does not address the requirement for "the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) in the solution are selected so that the material for forming the semiconductive layer and the material for forming the dielectric layer phase separate by self-organization to form an interface between the material for forming the semiconductive layer and the material for forming the dielectric layer" but merely makes reference to column 15.

Hirai

Hirai does not teach a solution in which two materials are in the same solution, namely (1) the materials for forming the semiconducting layer and (2) the materials for forming the dielectric layers. Moreover, Hirai does not teach that the semiconducting layer materials and the dielectric layer materials phase separate by self-organization.

Specifically, the reference in Hirai to a "self-organization, orientation layer between the gate insulating layer and the semiconductor channel" indicates that the gate insulating layers and semiconducting channel **are formed in separate deposition steps**.

There is no teaching or suggestion that any portion of Hirai teaches the formation of two layers as a result of a single deposition step.

Basic Patent Law provides with respect to rejections under Section 102 that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). In the absence of the single deposition step for multiple materials that phase separate into different layers, the claim cannot be anticipated.

Claims 2, 4-12, 14-17, 20 and 21

These claims, which depend from allowable claim 1, would be patentable for reasons given for claim 1.

Claim 23

In framing the rejection of independent claim 23, the Examiner again refers to column 15 of Hirai for a teaching of a step of "depositing on the first electrode a layer of a solution containing material for forming the semiconductive layer and material for forming the dielectric layer," where "the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) in the solution are selected so that the material for forming the semiconductive layer and the material for forming the dielectric layer phase separate by self-organisation to form an interface between the material for forming the semiconductive layer and the material for forming the dielectric layer."

Hirai is deficient in teaching the claimed single step deposition of two materials, as

previously noted for claim 1. Further, Hirai teaches away from a single step deposition, as Hirai is focused only on a two step deposition. Not only is this two-step process contrary to the approach taken by the present invention, it loses all of the advantages of a single step process. In the absence of the teaching of the claimed deposition step, the clam cannot be anticipated.

Claims 24 and 25

These claims, which depend from allowable claim 23, would be patentable for reasons given for claim 23.

Claim Rejections - 35 USC § 103

Claims 3, 13, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai (US 7037767 B2). This rejection is traversed for at least the following reasons.

These claims, which depend from allowable claim 1, would be patentable for reasons given for claim 1.

Moreover, Hirai in fact teaches away from the claimed idea of a single deposition step for the semiconducting and dielectric layers, involving depositing a layer of a solution containing both the material for the semiconducting layer and the material for forming the dielectric layer, and controlling conditions such that the two materials phase separate to form the semiconducting and dielectric layers.

Thus, applying the *Graham* and *KSR* standards, none of the rejected claims would be unpatentable over Hirai.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai (US 7037767 B2) in view of Veres (US 7029945 B2). This rejection is traversed for at least the following reasons.

This claim, which depends from allowable claim 1, would be patentable for reasons given for claim 1. Veres does not remedy the deficiencies of Hirai, as it is cited only for a teaching of a top gate transistor configuration.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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